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10/601,104	06/19/2003	Terry R. Lee	501178.01	7033

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EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 07/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/601,104	LEE ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7,11-15,17-19,23-25,27-30,32-34,38-40,42-47,51-56 and 60* is/are rejected.

7)☒ Claim(s) *4, 8-10,16, 20-22,26,31,35-37,41,48-50,57-59 and 61* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12/23/03, 1/26/04, 2/24/04, 5/17/04, 1/3/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Specification

1. The disclosure is objected to because of the following informalities:

The reference to the processor (element 194) on page 9, line 8 of the specification should be changed to element 104.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 5-7, 11-15, 17-19, 23-25, 43-47, 51-56 and 60 are rejected under 35 U.S.C. 102(e) as being anticipated by Perego et al. (hereinafter Perego) US Patent 6,889,304 B2.

As for claims 1 and 13, Perego teaches a memory system (as in claim 13, and a memory module as in claim 1), comprising:

a controller operable to receive a memory request and to transmit a corresponding memory request to an input/output port (col. 1 lines 20-25, the controller communicates with the memory modules);

a plurality of memory modules (col. 1, lines 20-25), each of the memory modules comprising:

a plurality of memory devices arranged in a plurality of ranks (col. 4, lines 50-55 – each of the physical memory banks are combined to form logical banks, i.e. ranks);

and a memory hub (Fig. 3, data control circuit, element 315) operable to receive a memory request at an input/output port (Fig. 3, the I/Os (325)), the memory hub being coupled to the memory devices in each of the ranks (again, Fig. 3 illustrates the connection of the data control circuit, I/Os and logical banks (element 305)), the memory hub being programmable to configure the memory module in a plurality of data formats each corresponding to a respective number of ranks of memory devices that are simultaneously accessed (col. 4, lines 63-67 – the configuration logic controls the configuration of the memory core via the data control circuit); and

a communications link coupling the input/output port of the controller to the input/output ports of the memory hubs in the respective memory modules (not shown in Fig. 3, however the motherboard uses the controller to interface with the memory modules via the I/Os as shown in Fig. 3 (col. 1, lines 20-27).

As for claims 2 and 14, Perego teaches the memory module/system of claims 1 and 13 wherein the memory hub is coupled to the memory devices in each of the ranks through respective busses (referring to Fig 4A, the latch circuitry disclosed in element

320 illustrates the logical connections of each of the physical banks with the I/O circuitry. The data control circuit is connected to the latch circuitry as indicated in Fig. 3).

As for claims 3 and 15, Perego teaches the memory module/system of claims 1 and 13 wherein the memory hub is operable to either address all of the ranks of memory devices in a first mode to simultaneously couple data to or from all of the memory devices in the memory module, or address less than all of the ranks of memory devices in a second mode to couple data to or from less than all of the memory devices in the memory module (the data control circuit works in concert with the configuration logic to configure the memory – see col. 4, lines 60-67). As shown in Fig. 4, the latch circuitry (element 320) and configuration logic (element 310) work together in order to control the addressing of each of the logical banks – col. 4, lines 40-49 each of the physical banks contain an input and output latch in order to select all or some of the physical banks during read or write operations. In addition, note Perego also teaches limiting access to only selected banks for the purposes of improving power consumption (col. 6, lines 50-51).

As for claims 5 and 17, Perego teaches the memory module/system of claims 1 and 13 further comprising a programmable storage device coupled to the memory hub, the programmable storage device being programmed to control the operating mode of the memory hub (Fig. 3, element 310; the configuration logic device supplies the control circuit with the memory bank configurations – col. 4, lines 63-67).

As for claims 6 and 18, Perego teaches the memory module/system of claims 1 and 13 wherein the memory devices in each rank are collectively operable to read or write N-bit data words (col. 5, lines 37-39; the width (N) is determined by the number of banks), and wherein the memory hub further comprises an input/output port (Fig. 4A, element 325) that is operable to receive or transmit M*N-bit data words, where M is the number of ranks of memory devices in the memory module (the I/O uses either one, or more than one of the data terminals (D0-D3) depending on the width of the word).

As for claims 7 and 19, Perego teaches the memory modules/system of claims 1 and 13 wherein the memory devices in each rank are collectively operable to read or write N-bit data words (col. 5, lines 37-39; the width (N) is determined by the number of banks) in a first period of time, and wherein the memory hub further comprises an input/output port (Fig. 4A, element 325) that is operable to receive or transmit M*N-bit data bits in a first period of time, where M is the number of ranks of memory devices in the memory module (the I/O uses either one, or more than one of the data terminals (D0-D3) depending on the width of the word) Note the latches are used in conjunction with the control signals to determine how many bits are routed to the I/Os. The latching will occur during a first period of time (i.e. any given memory cycle). See col. 6, lines 11-30.

As for claims 11,12, 23 and 24, Perego teaches the memory modules/system of claims 1 and 13 as dynamic random access devices, more specifically a synchronous dynamic random access devices (SDRAM) (col. 3, lines 46-48).

As for claims 43 and 51, Perego teaches a method of accessing data in a memory module containing a plurality of memory devices, the method comprising:

dividing the memory devices into a plurality of ranks (col. 4, lines 50-52 – logical banks);

configuring the memory module to access the data stored in the memory module in a first data format in which a first number of ranks of memory devices are simultaneously accessed;

configuring the memory module to access the data stored in the memory module in a second data format in which a second number of ranks of memory devices are simultaneously accessed, the second number being different from the first (col. 5, lines 28-40 – the example illustrated uses four physical banks which can be either divided into one logical block, four bits wide; two logical blocks, two bits wide; or four logical blocks, one bit wide); and

accessing data in each of the memory modules in the configured data format (the data is simultaneously written to or read from the banks via the data terminals as shown in Table 1, col. 6).

As for claim 44, Perego teaches the method of claim 43 wherein the act of configuring the memory module to access the data stored in the memory module in the first data format comprises configuring the memory module to simultaneously access all of the ranks of memory devices in the memory module so that data are simultaneously coupled to or from all of the memory devices in the memory module (using the method described in col. 4, lines 50-63, Perego could arrange eight physical

banks into eight logical banks each consisting of one physical bank, therefore all ranks would be accessed simultaneously), and wherein the act of configuring the memory module to access the data stored in the memory module in the second data format comprises configuring the memory module to individually access each of the ranks of memory devices in the memory module so that data are simultaneously coupled to or from only the memory devices in a single rank of memory devices (again, using the method described in col. 4, lines 50-63, Perego could arrange eight physical banks into one logical bank, therefore memory would be accessed as one single rank at a time).

As for claim 45, Perego teaches the method of claim 43, further comprising configuring the memory module to simultaneously access a plurality but less than all of the ranks of memory devices in the memory module so that data are simultaneously coupled to or from all of the memory devices in a plurality of ranks of memory devices but less than all of the memory devices in the memory module (col. 5, lines 17-27 – multiplexing logic can allow all (four in this example) data lines to be routed from the banks, or less than all bank (for example two as described in his teachings).

As for claims 25, and 60, Perego teaches the memory system of claim 13, and method in claim 51, wherein the memory hubs in at least two of the memory modules are programmed to configure the memory module in different data format. Note in col. 1, lines 38-54 the draw backs of using memory with statically sized memory widths are described. Perego's claimed invention aims to provide a means for dynamically adjusting the width of data based on application. Also note that Perego describes a plurality of memory modules in his system (col. 5, lines 7-15 (each memory slice is a

module)). Perego's system allows for more than one memory format since it supports more than one memory module at a time simultaneously.

As for claims 46 and 55, Perego teaches the method of claims 43 and 51 wherein the memory devices in each rank are collectively operable to read or write N-bit data words, and wherein the method further comprises receiving or transmitting M*N-bit data words from the memory module, where M is the number of ranks of memory devices in the memory module (col. 5, lines 37-39; the width (N) is determined by the number of banks. Further the I/O uses either one, or more than one of the data terminals (D0-D3) depending on the width of the word). All the possible read/write commands are illustrated in col. 6, Table 1 for the example uses four physical banks.

As for claims 47 and 56, Perego teaches the method of claims 43 and 51 wherein the memory devices in each rank are collectively operable to read or write N-bit data words (col. 5, lines 37-39; the width (N) is determined by the number of banks) in a first period of time, and wherein the method further comprises receiving at the memory module or transmitting from the memory module M N-bit data bits in a first period of time, where M is the number of ranks of memory devices in the memory module. Again, col. 5, lines 35-40 describe for example four physical banks arranged as two two-physical bank logical banks (each consisting of two bits). Data across the DQs are transmitted as two, two-bit words.

As for claim 52, Perego teaches the method of claim 51 wherein the act of configuring the memory modules to access the data stored in the memory modules in one of a plurality of data formats comprises configuring at least one of the memory

modules to simultaneously access all of the ranks of memory devices in the memory module so that data are simultaneously coupled to or from all of the memory devices in the memory module (col. 4, lines 60-62 – in this example Perego teaches combining all eight physical banks into one logical bank in order to access all of the memory in an 8-bit wide format).

As for claim 53, Perego teaches the method of claim 51 wherein the act of configuring the memory modules to access the data stored in the memory modules in one of a plurality of data formats comprises configuring at least one of the memory modules to individually access each of the ranks of memory devices in the memory module so that data are simultaneously coupled to or from only the memory devices in a single rank of memory devices. Again, as stated above, by configuring his system into one logical bank consisting of eight physical banks, Perego is able to individually access one and only one rank at time (col. 4, lines 60-62).

As for claim 54, Perego teaches the method of claim 51 wherein the act of configuring the memory modules to access the data stored in the memory modules in one of a plurality of data formats comprises configuring at least one of the memory modules to simultaneously access a plurality but less than all of the ranks of memory devices in the memory module so that data are simultaneously coupled to or from all of the memory devices in a plurality of ranks of memory devices but less than all of the memory devices in the memory module. In col. 6, lines 51-67, Perego describes using bank-select signals to determine which banks to access. This allows Perego to only select some of the banks during a read or write operation. By using the

method described in col. 4, lines 50-63, Perego could arrange eight physical banks into four logical banks of two physical banks. The bank-select signals could be used to read only two of the four logical banks.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 28-30, 32-34 and 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pax (US PG Publication 2003/0227798 A1) and further in view of Perego.

As for claim 28, Pax discloses a reduced power memory module and method, which includes a processor (Fig. 3, element 60), a system controller (Fig. 3, element 68) coupled to the CPU, the system controller being operable to receive a memory request from the CPU and to transmit a corresponding memory request (the control bus allows command signals, i.e. memory requests to be transmitted between the CPU and controller, Fig. 3, element 64 – paragraph 0014, lines 1-14). Pax further teaches an input device (Fig. 3, element 66), and output device (Fig. 3, element 70), and a storage device (Fig.3, element 74) coupled to the controller.

Perego teaches a plurality of memory devices arranged in a plurality of ranks (col. 4, lines 50-55 – each of the physical memory banks are combined to form logical banks, i.e. ranks);

and a memory hub (Fig. 3, data control circuit, element 315) operable to receive a memory request at an input/output port (Fig. 3, the I/Os (325)), the memory hub being coupled to the memory devices in each of the ranks (again, Fig. 3 illustrates the connection of the data control circuit, I/Os and logical banks (element 305)), the memory hub being programmable to configure the memory module in a plurality of data formats each corresponding to a respective number of ranks of memory devices that are simultaneously accessed (col. 4, lines 63-67 – the configuration logic controls the configuration of the memory core via the data control circuit); and

a communications link coupling the input/output port of the controller to the input/output ports of the memory hubs in the respective memory modules (not shown in Fig. 3, however the motherboard uses the controller to interface with the memory modules via the I/Os as shown in Fig. 3 (col. 1, lines 20-27).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Pax to further include Perego's system of a memory device with a dynamically configurable core. By doing so, Pax would be able to further improve his system of reducing power consumption (Perego, col. 4, lines 25-45) by dynamically

adjusting the groupings of SDRAM (Pax -- Fig. 3, elements 90, 92, 94, etc) based on adjustable logical bank widths as taught by Perego.

Claims 29, 30, 32, 33, 34 and 38-40 are rejected for the reasons as described in claims 2, 3, 5, 6, 7,11,12 and 25 above respectively.

4. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Perego as applied to claim 13 above, and further in view of Updegrove, US Patent 6,233,376 B1.

As for claim 27, though Perego fails to teach all of the limitations of this claim, he fails to disclose the I/O port of the hub being comprised of an optical I/O port, further they fail to teach the communications link as being comprised of an optical communications link. Updegrove however teaches a system which includes fiber optic circuit boards for integrated circuits. His teachings include the benefits of fiber optic conductors to overcome bandwidth and data rate limitations of conventional printed circuit boards (col. 1, lines 46-51).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Perego to further incorporate Updegrove's system for fiber optic circuit boards and integrated circuits as described in col. 1, lines 20-26 of Perego's teachings (replacing the conductive traces of the motherboard with optical). By doing so, Perego's system would benefit from the increased bandwidth and data rate as taught by Updegrove (col. 1, lines 46-51).

5. Claim 42 is under 35 U.S.C. 103(a) as being unpatentable over Pax in further view of Perego as applied to claims 28 above, and further in view of Updegrove.

Claim 42 is rejected for similar reasons as provided for claim 27.

Allowable Subject Matter

6. Claims 4, 8-10, 16, 20-22, 26, 31, 35-37, 41, 48-50, 57-59 and 61 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

As for claims 4, 16, 26, 31, 41 and 61, though Perego teaches configuring a memory module, and also provides teachings for multiple memory modules within his system, he fails to specifically teach each of the three configurations as described by applicant.

As for claims 8-10, 20-22, 35-37, 48-50, and 57-59, Perego fails to teach reading or writing data at any particular rate. In addition, he fails to specifically teach his I/O as transmitting or receiving N-bit data words at a rate of M*X data words per second.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Baker et al. (US PG Publication 2003/0043426 A1) discloses an optical interconnect in high-speed memory systems.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

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REGINALD G. BRAGDON
PRIMARY EXAMINER